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(54) Semiconductor chip stack and method for manufacturing the same

(57) A semiconductor chip having a plurality of device formative layers that are formed into an integrated thin film is provided by a technique for transferring. According to the present invention, a semiconductor chip that is formed into a thin film and that is highly integrated can be manufactured by transferring a device formative layer (501) with a thickness of at most 50μm which is separated from a substrate (322) into another substrate by a technique for transferring, and transferring another device formative layer with a thickness of at most 50μm which is separated from another substrate to the above device formative layers, and, repeating such transferring process.

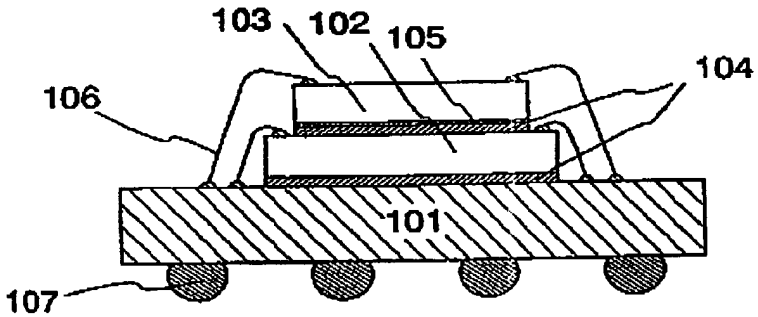

Fig. 1A

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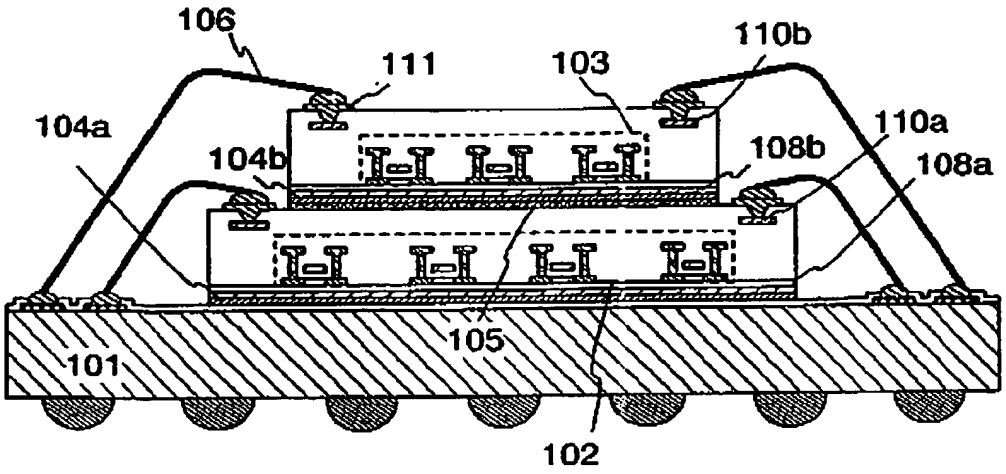

Fig. 1B

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a semiconductor chip and a manufacturing method for the semiconductor chip manufactured by stacking a plurality of device formative layers which includes a semiconductor apparatus, a display apparatus, and a light-emitting apparatus each of which is composed of a plurality of thin film transistors (hereinafter, TFTs) over a substrate. The above described semiconductor apparatus includes a CPU, (Central Processing Unit), an MPU (Micro Processor Unit), a memory, a microcomputer, and an image processor. The above described display apparatus includes a liquid crystal display apparatus, PDP (Plasma Display Panel), FED (Field Emission Display), or the like. The above described light-emitting apparatus includes an electroluminescent apparatus or the like.

2. Related Art

[0002] In recent years, a technique for fabricating a TFT using a semiconductor thin film (having a thickness of from approximately several to several hundreds nm) fabricated over a substrate having an insulating surface has been attracted attention. A TFT is widely utilized for an electronic device such as an IC, an optical device, or the like.

[0003] However, there has been a problem that a requirement for a substrate that is used while forming a TFT and a requirement for a substrate that is used after forming a TFT are not same.

[0004] For instance, as a substrate for forming a TFT, a glass substrate or a quartz substrate is widely used now since these substrates have high heat-resistance so that they can be used when the process temperature is high, however, these substrates have some disadvantages such as being fragile and heavy.

[0005] On the other hand, a flexible substrate such as a plastic film, although it cannot be used in the process at a high temperature for its low heat-resistance, has advantages such as hardly being cracked and being lightweight. However, a TFT formed in the process at a low temperature cannot obtain greater electric characteristics than that formed over a glass substrate or a quartz substrate.

[0006] As a technique that utilizes merits of using these both substrates, a technique for fabricating a thin film device over a glass substrate or a quartz substrate, and separating the thin film device (separated body) from the substrate, and then transferring to a transferred body such as a plastic substrate, etc are disclosed. (For example, Japanese Laid-Open Patent Application No. 10-125929.)

[0007] According to this, a thin film device can be formed over various substrates no matter what process the thin film device went through by using the technique for separating and transferring the thin film device to another substrate.

[0008] In the field of LSI, various ways for manufacturing a high-integrated semiconductor apparatus has been proposed, for example, a technique for packaging a semiconductor device in three dimensions by stacking a plurality of chips is known. (For example, Japanese Laid-Open Patent Application No. 6-244360)

[0009] However, a stacked semiconductor chip is expected to be formed into a further thinner film in realizing its high performance, its high operation, and its miniaturization since there is a technical limit in forming the semiconductor chip into a thin film.

SUMMARY OF THE INVENTION

[0010] In view of the foregoing, it is an object of the present invention to provide a semiconductor apparatus in which a plurality of device formative layers formed into a thin film over a substrate (including a semiconductor apparatus (a CPU, an MPU, a memory, a microcomputer, an image processor, or the like) , a display apparatus (a liquid crystal display apparatus, a PDP, a FED, or the like), or a light-emitting apparatus) are integrated.

[0011] A further object of the present invention is to form a structure that prevents each device from deteriorating due to accumulated heat generated in each device formative layer in case of integrating a plurality of device formative layers over a substrate.

[0012] According to the present invention, a semiconductor chip that is higher integrated and that is formed into a thinner film compared with the conventional semiconductor chip packaged in three dimensions can be realized by transferring a device formative layer with a thickness of at most 50μm which is separated from a substrate to another substrate by using a technique for transferring, and transferring another device formative layer with a thickness at most 50μm which is separated from another substrate to the above device formative layer, and repeating such transferring process.

[0013] In the present invention, a substrate is characterized by being formed of a thermal conductive material that can radiate heat effectively in consideration of the fact that a device formative layer serving as a transferred body has a thickness of at most 50μm and a device is easily deteriorated due to heat generated in the device formative layer. In addition, a thermal conductive thin film is preferably fabricated over the surface of a transferred body (over the transferred device formative layer) in case of transferring another device formative layer to the transferred device formative layer.

[0014] As used herein, the term "thermal conductive substrate" refers to a substrate formed of a ceramic material containing aluminum oxide (alumina), aluminum nitride, aluminum nitride oxide, silicon nitride, or the like as its main components, and a graphite material con-

taining carbon as its main components. As used herein, the term "thermal conductive thin film" refers to a thin film of aluminum nitride (AlN), aluminum nitride oxide ($AlN_XO_Y(X>Y)$, boron phosphide (BP), or diamond like carbon (DLC: Diamond Like Carbon), or a lamination film or the like of these films.

[0015] The lamination structure according to the present invention, with respect to the electric interconnection in a lateral direction, is characterized by the flip chip structure in which wirings (auxiliary wirings) are formed into each device formative layer in advance, and the wirings are connected electrically to the wirings in the other device formative layer when these device formative layers are stacked and bonded each other in a lateral direction, in addition to a wire bonding structure in which terminals provided in a part of each layer are connected each other by connection wires.

[0016] A method for separating or transferring used in the present invention is not especially limited. For example as the method for separating or transferring, a metal layer (or a metal nitride layer) is fabricated over a substrate, a metal oxide layer is fabricated thereon, and an oxide layer is fabricated in contact with the metal oxide layer, and then, a device is formed over the oxide layer, subsequently, the device is separated from the substrate by splitting-off the metal oxide layer or an interface between the metal oxide layer and another layer. In addition, in order to improving the way of separating, a heat treatment or a laser light irradiation may be carried out. Or it is possible that a film containing hydrogen is fabricated over the oxide layer and a heat treatment is carried out on the resulted film to crystallize metal oxides. Further, a stress peel-off method may be adopted by which a film is separated utilizing membrane stress between two layers.

[0017] In addition, a method for separating by which a device formative layer and a substrate are separated by means of fabricating a layer for separating between the device formative layer and the substrate and removing the resulted layer by etchant can be adopted. Further, a method for separating by which a device formative layer and a substrate are separated by means of fabricating an amorphous silicon layer (or a polysilicon layer) between the device formative layer and the substrate and by irradiating laser light to the resulted amorphous silicon layer through the substrate can also be adopted.

[0018] The constitution according to the present invention is a semiconductor chip having a structure in which a plurality of device formative layers having thicknesses of at most 50μm is fabricated over a substrate having thermal conductivity.

[0019] A semiconductor chip having a plurality of devices formative layers with thicknesses of at most 50μm over a thermal conductive substrate, comprising:

a first device formative layer with a thickness of at most 50μm fabricated over the thermal conductive substrate via a first adhesive layer;
a thermal conductive film fabricated in contact with the first device formative layer; and
a second device formative layer with a thickness of at most 50μm fabricated over the thermal conductive film via a second adhesive layer.

[0020] The device formative layer (the first device formative layer and the second device formative layer) in the above constitution is preferably has a thickness of from 0.1 to 10μm.

[0021] In the above constitution, a semiconductor device included in the first device formative layer and a semiconductor device included in the second device formative layer are electrically connected each other via connection wires by wirings included in the first device formative layer and wirings included in the second device formative layer.

[0022] In another constitution, a semiconductor device included in the first device formative layer and a semiconductor device included in the second device formative layer are electrically connected each other via the first and second adhesive layers containing an anisotropic conductive material by connection wires connected to each wirings included in the first device formative layer and wirings included in the second formative layer.

[0023] As an anisotropic conductive material, metallic particles such as Ag, Au, Al, or the like coated with insulating films and having a unidirectional conductivity can be used. In case of using anisotropic conductive materials for bonding the first and second device formative layers, it is preferably to irradiate the device formative layers with ultra waves to strengthen their adhesiveness

[0024] In the present invention, the device formative layer is not limited to have one layer. The number of the device formative layer can be increased by stacking sequentially a film having thermal conductivity and a device formative layer as in the case with the second device formative layer.

[0025] The device formative layer includes TFTs, a semiconductor apparatus formed by combining these TFTs (a CPU, an MPU, a memory, a microcomputer, an image processor, or the like), a display apparatus (a liquid crystal display apparatus, a PDP, a FED, or the like), or a light-emitting apparatus.

[0026] The constitution of the present invention is a method for manufacturing a semiconductor chip having a plurality of device formative layers with thicknesses of at most 50μm over a thermal conductive substrate for obtaining a semiconductor chip that is integrated without increasing the area by stacking sequentially device formative layers with thicknesses of at most 50μm over a thermal conductive substrate, comprising the steps of:

fabricating a first device formative layer including a plurality of thin film transistors over a first substrate;

fabricating a soluble organic resin film over the first device formative layer;
fabricating a first adhesive layer in contact with the first soluble organic resin film;
bonding the second substrate to the first soluble organic resin film via the first adhesive layer, and sandwiching the first device formative layer and the first soluble organic resin film between the first substrate and the second substrate;
separating and removing the first substrate from the first device formative layer by a physical means;
fabricating a second adhesive layer in contact with the thermal conductive substrate;
bonding an exposed surface of the first device formative layer to the thermal conductive substrate via the second adhesive layer;
separating the first adhesive layer and the second substrate from the first device formative layer;
removing the first soluble organic resin film with solvent;
fabricating a thin film having thermal conductivity over an exposed surface;
fabricating a second device formative layer including a plurality of thin film transistors over a third substrate;
fabricating a second soluble organic resin film over the second device formative layer;
fabricating a third adhesive layer in contact with the second soluble organic resin film;
bonding the fourth substrate to the second soluble organic resin film via the third adhesive layer, and sandwiching the second device formative layer and the second soluble organic resin film between the third substrate and the fourth substrate;
separating and removing the third substrate from the second device formative layer by a physical means;
fabricating a fourth adhesive layer in contact with a thin film having thermal conductivity; and
an exposed surface of the second device formative layer over the thin film having thermal conductivity via the fourth adhesive layer.

[0027] In the above constitution, the thin film having thermal conductivity is formed of a film of aluminum nitride, aluminum nitride oxide, boron phosphide, boron nitride, or diamond like carbon, or a lamination film of these films, each of which is formed by sputtering.

[0028] Further, in the above constitution, either or both of the second adhesive layer and the fourth adhesive layer are fabricated by using an anisotropic adhesive, and the device formative layer is bonded via either or both of the second adhesive layer and the fourth adhesive layer by being irradiated with ultra waves.

[0029] In the above each constitution, the constitution in which a metal layer, a metal oxide layer, and an oxide layer are fabricated sequentially over a first substrate and a third substrate to form a metal oxide having a crystal structure within the metal oxide layer for separating and removing the first easily substrate and the third substrate by a physical means of splitting-off the metal oxide layer is included. Further, the constitution in which the metal oxide layer having a crystal structure is fabricated by fabricating a film containing hydrogen (a silicon nitride film, a silicon nitride oxide film, an amorphous semiconductor film, or the like) over the oxide layer and heat-treating the resulted film for dispersing hydrogen is included in the above each constitution.

[0030] For separating easily the first substrate or the third substrate, reinforcing substrates can be bonded to each the first substrate or the third substrate via adhesive layers. The reinforcing substrate can be separated together with the first substrate or the third substrate.

[0031] According to the present invention, a semiconductor chip can be formed into a thinner film and a higher integrated semiconductor chip by stacking a plurality of device formative layers with thicknesses of at most 50μm over a thermal conductive film by a technique for transferring compared with the case of packaging the device formative layers in three dimension. The problems arisen in case of stacking a plurality of thin device formative layers that the heat accumulation and the deterioration of a device due to the accumulated heat can be prevented by interposing thermal conductive layers between the laminated device formative layers.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032]

Figs. 1A to 1C are explanatory views of the structure of a semiconductor chip according to the present invention;
Figs. 2A to 2C are explanatory views of the structure of a semiconductor chip according to the present invention;
Figs 3A to 3C are explanatory views of a method for manufacturing a semiconductor chip according to the present invention;
Figs 4A to 4C are explanatory views of a method for manufacturing a semiconductor chip according to the present invention;
Figs 5A to 5C are explanatory views of a method for manufacturing a semiconductor chip according to the present invention;
Figs 6A to 6C are explanatory views of a method for manufacturing a semiconductor chip according to the present invention;
Figs. 7A to 7C are explanatory views of a method for manufacturing a semiconductor chip according to the present invention;
Figs. 8A to 8C are explanatory views of a method for manufacturing a semiconductor chip according to the present invention;
Figs. 9A and 9B are explanatory views of the structures of semiconductor chips according to the

present invention;

Fig. 10 is an explanatory view of a structure of a CPU included in a semiconductor chip according to the present invention;

Fig. 11 is an explanatory view of the embodiment of a semiconductor chip according to the present invention;

Figs. 12A to 12$_D$ are explanatory views of a manufacturing process of TFTs;

Figs. 13A to 13D are explanatory views of a manufacturing process of TFTs;

Fig. 14 is an explanatory view of a module incorporated with a semiconductor chip according to the present invention;

Figs. 15A to 15G are explanatory views of electric appliances utilizing a semiconductor chip according to the present invention;

Figs. 16A and 16B are explanatory views of a bottom gate TFT and a dual gate TFT;

Figs. 17A and 17B are explanatory views of a method for manufacturing a semiconductor chip according to the present invention; and

Figs. 18A and 18B are explanatory views of a method for manufacturing a semiconductor chip according to the present invention.

DESCRIPTION OF THE PREFFERED EMBODIMENTS

[0033] Hereafter, embodiment modes of the present invention will be described.

Embodiment Mode 1

[0034] The structure of a semiconductor chip manufactured according to the present invention is explained with reference to Figs. 1A to 1C. As shown in Fig. 1A, the semiconductor chip according to the present invention has a wire bonding structure in which a first device formative layer 102 is stacked over thermal conductive substrate 101 interposing an adhesive layer 104, and a second device formative layer 103 is stacked thereon interposing an adhesive layer 104. then, wirings (not shown) of each the first device formative layer 102 and the second device formative layer 103 are connected electrically to wirings (not shown) of the thermal conductive substrate 101 by connection wires 106.

[0035] The device formative layers (the first device formative layer 102 and the second device formative layer 103) have thicknesses at most 50μm. Further, these device formative layers were fabricated in advance over another substrate and separated from the substrate by a technique for separating.

[0036] A substrate having thermal conductivity (the thermal conductive substrate 101) is used for the substrate on which the first device formative layer 102 is pasted since the device formative layer according to the present invention is a thin film having a thickness of at most 50μm and a device is susceptible to generated heat. In case of fabricating the second device formative layer 103 over the first device formative layer 102 via the adhesive layer 104, a thermal conductive film 105 is fabricated in contact with the first device formative layer 102. In addition, a flattening film may be fabricated over the surface of the thermal conductive substrate 101 for preventing device destruction or interconnection destruction in the first device formative layer 102 or the second device formative layer 103, which are thin films, due to irregularities (not shown) of the surface of the thermal conductive substrate 101.

[0037] As the thermal conductive substrate 101, a ceramic substrate containing aluminum oxide (alumina), aluminum nitride (AlN), aluminum nitride oxide (AlN_XO_Y (X>Y), silicon nitride, or the like as its main components, and a graphite substrate containing carbon as its main components can be used. As the thermal conductive film 105, a film of aluminum nitride (AlN), aluminum nitride oxide (AlN_XO_Y(X>Y), boron phosphide (BP), boron nitride (BN), diamond like carbon (DLC: Diamond Like Carbon) or a lamination film or the like of these films can be used.

[0038] A method for fabricating the thermal conductive film 105, sputtering, vapor deposition, CVD, or the like can be used.

[0039] For example, in case of fabricating the thermal conductive film 105 by AlN, the film is deposited by using aluminum nitride (AlN) target under the atmosphere composed of mixed gas of argon gas and nitride gas. In addition, the film can be deposited using aluminum (Al) target under the atmosphere of nitride gas.

[0040] Each the pasted first device formative layer 102 and second device formative layer 103 is electrically connected to the wirings (not shown) over the thermal conductive substrate by the connection wire 106 respectively. As a material for forming the connection wire, a wire formed of Au, Cu, Al, Al-Si, or an alloy of Au can be used

[0041] The first device formative layer 102 and the second device formative 103 can be electrically connected to the outside by bonding the wirings of the thermal conductive substrate to a printed wiring board (not shown) via a solder ball 107 connected electrically to the wirings of the thermal conductive substrate 101.

[0042] The structure of the device formative layer (the first device formative layer 102 and the second device formative 103) shown in Fig. 1A and electrical interconnection between the device formative layer and the thermal conductive substrate 101 by the connection wire 106 are explained with reference to Fig. 1B.

[0043] In the device formative layer 102, a plurality of thin film transistors (hereinafter, TFTs) are formed as semiconductor devices, and a semiconductor apparatus (a CPU, an MPU, a memory, a microcomputer, an image processor, or the like); a display apparatus (a liquid crystal apparatus, a PDP, an FED, or the like); or a light-emitting apparatus, each of which includes devices

formed by combining these TFTs, is manufactured.

[0044] The first device formative layer 102 includes an oxide layer 108a a part of which has a metal oxide layer since the device formative layer can be obtained as the following process: a plurality of TFTs and wirings (auxiliary wiring) are formed over a metal layer, a metal oxide layer, and an oxide layer fabricated over a substrate, and the oxide layer and TFTs formed over the oxide layer are separated from the substrate and the metal layer by splitting-off the metal oxide layer by a physical means. The oxide layer 108a a part of which has a metal oxide layer is bonded to the thermal conductive substrate 101 via an adhesive layer 104a.

[0045] As a material for forming the adhesive layer 104a, various curing adhesives such as a photo-curing adhesive, for example, a reaction-curing adhesive, a thermal-curing adhesive, or a UV-curing adhesive, or an anaerobic adhesive can be used.

[0046] The device formative layer 103 is fabricated over the first device formative layer 102 via the thermal conductive film 105.

[0047] The second device formative layer 103 includes an oxide layer 108b a part of which has a metal oxide layer since the device formative layer can be obtained as the following process: a plurality of TFTs and wirings (auxiliary wiring) are formed over a metal layer, a metal oxide layer, and an oxide layer fabricated over a substrate, and the oxide layer and TFTs formed over the oxide layer are separated from the substrate and the metal layer by splitting-off the metal oxide layer by a physical means. The oxide layer 108b a part of which has a metal oxide layer is bonded to the thermal conductive film 105 via an adhesive layer 104b.

[0048] As a material for forming the adhesive layer 104b, various curing adhesives such as a photo-curing adhesive, for example, a reaction-curing adhesive, a thermal-curing adhesive, or a UV-curing adhesive, or an anaerobic adhesive can be used.

[0049] The first device formative layer 102 and the second device formative layer 103 can electrically connect to the outside by wirings (110a, 110b) formed in each the first device formative layer 102 and the second device formative layer 103 via an electrode pad 111.

[0050] A semiconductor apparatus, a display apparatus, a light-emitting apparatus, or the like, each of which includes devices composed of a plurality of TFTs and is formed in the first device formative layer 102 and the second device formative layer 103, is electrically connected to the wirings formed over the thermal conductive substrate by the connection wire 106.

[0051] Although the case that the device formative layer is formed to have a two-lamination layer is explained in Embodiment Mode 1, but not exclusively, the device formative layer may be formed to have a three- or more-lamination layer.

[0052] Thus, a semiconductor chip having a structure in which a plurality of device formative layers are stacked over the thermal conductive substrate.

[0053] After forming the interconnection structure shown in Fig. 1B, a resin 112 may be formed to encapsulate the device formative layer (102, 103) and the connection wire 106. In addition, a material for the resin 112, a thermosetting resin or a thermoplastic resin can be used. Specifically, a mold resin such as an epoxy resin, a silicon resin, a PPS resin (polyphenylene sulfide resin), or the like can be used. In the present invention, a substrate formed of glass, quartz, plastic, or a metal material can be used instead of resin.

Embodiment Mode 2

[0054] The structure of a semiconductor chip that is different from that described in Embodiment Mode 1 will be described in Embodiment Mode 2. Figs. 1A to 1C illustrate the structure that the device formative layer is electrically connected to the thermal conductive substrate by the connection wire 106. In this embodiment, the case of adopting a flip chip structure in which laminated device formative layers are connected electrically to a thermal conductive layer without using connection wires will be described.

[0055] As shown in Fig. 2A, a first device formative layer 202 having a thickness at most 50μm is stacked over a thermal conductive substrate 201 via an anisotropic conductive layer 204, and a second device formative layer 203 having a thickness at most 50μm is stacked over the first conductive layer 202 via an anisotropic conductive layer 203. Here, wirings are exposed over the surface of each the first device formative layer 202 and the second device formative layer 203, these wirings are electrically connected each other via the anisotropic conductive layer 204, and also electrically connected to the wirings (not shown) over the thermal conductive substrate.

[0056] The first device formative layer 202 and the second device formative 203 can be electrically connected to the outside by bonding the wirings of the thermal conductive substrate 201 to a printed wiring board (not shown) via a solder ball 206 connected electrically to the wirings of the thermal conductive substrate 201.

[0057] Here, the structure of the device formative layer (the first device formative layer 202 and the second device formative 203) shown in Fig. 2A and electrical interconnection between the device formative layer and the thermal conductive substrate 201 by auxiliary wirings a and b (210a and 210b) are explained with reference to Fig. 2B.

[0058] In the first device formative layer 202, a plurality of thin film transistors (hereinafter, TFTs) is formed as a semiconductor device, and a semiconductor apparatus composed of the TFTs (a CPU, an MPU, a memory, a microcomputer, an image processor, or the like); a display apparatus (a liquid crystal apparatus, a PDP, an FED, or the like); or a light-emitting apparatus, each of which includes these devices formed by combining these TFTs, is manufactured.

[0059] The separated surface of first device formative layer 202 includes an exposed oxide layer 208a and a part of an auxiliary wiring a (210a) since the first device formative layer 202 can be obtained as the following process: a plurality of TFTs and wirings (auxiliary wiring) are formed over a metal layer, a metal oxide layer, and an oxide layer fabricated over a substrate, and the oxide layer and TFTs formed over the oxide layer are separated from the substrate and the metal layer by splitting-off the metal oxide layer by a physical means, then, the auxiliary wiring a (210a) for reaching a wiring 209a is formed over the separated surface. The oxide layer 208a and the auxiliary wiring a (210a) are bonded to the thermal conductive substrate 201 via the anisotropic adhesive layer 204a. Thus, the auxiliary wiring a (210a) formed over the first device formative layer 202 is connected electrically to the wiring (not shown) over the thermal conductive substrate 201 via the anisotropic conductive adhesive layer 204a.

[0060] As a material for fabricating the anisotropic conductive adhesive layer 204a, an anisotropic conductive adhesive, which is made by dispersing an anisotropic conductive material on a photo-curing adhesive such as a reaction-curing adhesive, a thermal-curing adhesive, or a UV-curing adhesive, or an anaerobic adhesive, can be used. As an anisotropic conductive material, metal particles such as Ag, Au, Al, or the like coated with insulating films and having a unidirectional conductivity can be used. In case of using an anisotropic conductive, it is preferably to bond the first device formative layer with irradiating ultrasonic waves for obtaining the strong adhesiveness.

[0061] The second device formative layer 203 is stacked over the first device formative layer 202 via the thermal conductive film 205.

[0062] The separated surface of second device formative layer 203 includes an exposed oxide layer 208b and a part of an auxiliary wiring a (210b) since the device formative layer can be obtained as the following process: a plurality of TFTs and wirings (auxiliary wiring) are formed over a metal layer, a metal oxide layer, and an oxide layer fabricated over a substrate, and the oxide layer and TFTs formed over the oxide layer are separated from the substrate and the metal layer by splitting-off the metal oxide layer by a physical means, then, the auxiliary wiring a (210b) for reaching a wiring 209 is formed over the separated surface. The oxide layer 208b and the auxiliary wiring a (210b) are connected to the first device formative layer 202 via the anisotropic adhesive layer 204b. Thus, the auxiliary wiring a (210b) and the wiring 209b formed over the first device formative layer 202 are electrically connected via the anisotropic conductive adhesive layer 204b, moreover, connected electrically to wirings (not shown) formed over the thermal conductive substrate 201.

[0063] As a material for fabricating the anisotropic conductive adhesive layer 204b, an anisotropic conductive adhesive, which is made by dispersing an anisotropic conductive material on a photo-curing adhesive such as a reaction-curing adhesive, a thermal-curing adhesive, or a UV-curing adhesive, or an anaerobic adhesive, can be used. As an anisotropic conductive material, a metal particle such as Ag, Au, Al, or the like coated with an insulating film and having a unidirectional conductivity can be used. In case of using an anisotropic conductive, it is preferably to bond the second device formative layer with irradiating ultrasonic waves for obtaining the strong adhesiveness.

[0064] Fig. 2C is an enlarged view showing reference numeral 213 in Fig. 2B. Thus, the auxiliary wiring b (210b) formed in the second formative layer 202 and the wiring 209b formed in the first device formative layer 202 are electrically connected each other via an anisotropic conductive particle 215 within the anisotropic conductive adhesive layer 204b composed of the anisotropic conductive particle 215 and an adhesive 214. Here, the anisotropic conductive particle 215 has the structure in which metallic particles are coated with insulating films.

[0065] Therefore a semiconductor apparatus, a display apparatus, a light-emitting apparatus, or the like, each of which includes a device composed of a plurality of TFTs and is formed in the first device formative layer 202 and the second device formative layer 203, is electrically connected to the wirings formed over the thermal conductive substrate by the auxiliary wirings a and b (210a and 210b) and the anisotropic conductive adhesive layers (204a, 204b).

[0066] The case that the device formative layer is formed to have a two-lamination layer is explained in Embodiment Mode 2, but not exclusively, the device formative layer may be formed to have a three- or more-lamination layer.

[0067] Thus, a semiconductor chip having a structure in which a plurality of device formative layers are stacked over the thermal conductive substrate.

[0068] A top gate TFT is explained as an example of the type of a TFT in Embodiment Mode 1 and Embodiment Mode 2 in the present invention, but not exclusively, a bottom gate TFT having a structure in which a gate electrode is formed on the underside of an active layer as shown in Fig. 16A, or a dual gate TFT having a structure in which two gate electrodes are formed so as to sandwich an active layer as shown in Fig. 16B can be also adopted.

Embodiments

[0069] Hereinafter, Embodiments of the present invention will be described.

Embodiment 1

[0070] In this embodiment, a method for manufacturing a semiconductor chip according to the present invention, which has a structure explained in Embodiment Mode 1, will be described with reference to Figs. 3A to

5C.

[0071] Fig. 3A is a view of showing a state that a metal layer 301, a metal oxide layer 302, and an oxide layer 303 are sequentially fabricated over a first substrate 301, and a device formative layer 250 is fabricated thereon.

[0072] As the first substrate 300, a glass substrate, a quartz substrate, a ceramic substrate, a silicon substrate, a metal substrate, or a stainless substrate, or the like, can be used. In this embodiment, AN 100 which is a glass substrate, is utilized.

[0073] As materials for the metal layer 301 fabricated over the first substrate 300, an element selected from the group consisting of W, Ti, Ta, Mo, Nd, Ni, Co, Zr, Zn, Ru, Rh, Pd, Os, Ir, and Pt; a single layer fabricated of an alloy material or a compound material containing these elements as its main components; a lamination layer of the single layers; or nitrides, for example, a single layer or a lamination layer fabricated of titanium nitride, tungsten nitride, tantalum nitride, or molybdenum nitride. The metal layer 301 is fabricated to have a thickness of from 10 to 200nm, preferably, from 50 to 75nm.

[0074] In case of forming a metal layer 301 by sputtering, the thickness at the vicinity of its periphery portion of the first substrate 300 is tend to be inhomogeneous since the first substrate 300 is fixed. Therefore, it is preferable that only the periphery portion is removed by dry etching. In this regard, an insulating film fabricated of an oxynitride silicon film may be fabricated to have a thickness of approximately 100nm between the first substrate 300 and the metal layer 301 to prevent the first substrate 300 from being etched.

[0075] The metal oxide layer 302 and the oxide layer 303 are fabricated over the metal layer 301. In this embodiment, the case that the oxide layer 303 is fabricated, and the metal layer 301 is oxidized in the following process, and then, these layers are formed into the metal oxide layer 302 will be described.

[0076] Therefore a layer fabricated of tungsten is fabricated to have a thickness of from 10 to 200nm, preferably, from 50 to 75nm as the metal layer 301. Further, the oxide layer 303, here a silicon oxide layer, is stacked thereon to have a thickness of from 150 to 200nm without exposing to the atmosphere. The thickness of the oxide layer 303 is preferably more than twice as large as that of the metal layer 301. For example, a silicon oxide film is preferably fabricated to have a thickness of from 150 to 200nm by sputtering using silicon oxide targets.

[0077] A device formative layer 250 fabricated over the oxide layer 303 is the layer in which a semiconductor apparatus, a display apparatus, or a light-emitting apparatus including a device formed by combining appropriately TFTs (p-channel TFTs or n-channel TFTs) is formed. The TFT described here is composed of an impurity region 304, a channel formation region 306, each of which is formed in a part of a semiconductor film over a base film 305a, a gate insulating film 307, and a gate electrode 308, and is connected electrically by a wiring 309. Further, an electrode pad 310 which makes it possible to connect to the outside is formed

[0078] In the process for fabricating the device formative layer 250, heat treatment is carried out after forming a material film containing hydrogen at least (a semiconductor film or a metal film) to diffuse the hydrogen contained in the material film. The heat treatment may be carried out at least 420°C. The heat treatment may be carried out separately from the process for fabricating the device formative layer 250, or carried out simultaneously for simplification of processes. For example, in case of fabricating an amorphous silicon film containing hydrogen as a material film containing hydrogen by sputtering and heating the amorphous silicon film to form a polysilicon film, hydrogen in the amorphous silicon film can be diffused by the heat treatment at least 500°C simultaneously with forming a polysilicon film by the heat treatment.

[0079] According to the heat treatment, the metal oxide layer 302 having a crystal structure is fabricated between the metal layer 301 and the oxide layer 303. An amorphous metal oxide layer (tungsten oxide layer) with a thickness of from 2 to 5nm fabricated between the metal layer 301 and the oxide layer 303 by stacking the metal layer 301 and the oxide layer 303 is included in the metal oxide layer 302 since the metal oxide layer (tungsten oxide layer) is formed to have a crystal structure by this heat treatment.

[0080] In this embodiment, the case that the metal oxide layer 302 is fabricated in the process for manufacturing a part of a device formative layer is explained, but not exclusively, the metal oxide layer 302 may be formed after forming the oxide layer 301, and the oxide layer 303 may be formed thereafter.

[0081] Next, an organic resin layer 311 is fabricated over the device formative layer 250. As a material for fabricating the organic resin layer 311, an organic material that is soluble in water or alcohol is used. The organic resin layer 311 is fabricated by coating the organic material over the whole surface and curing. The organic material may be composed of, for example, epoxy series, acrylate series, silicon series, or the like. Specifically, water-soluble resin (TOAGOSEI Co., Ltd.: VL-WSHL10) is spin-coated to have a thickness of 30μm, and exposed for two minutes to be partially cured, then, exposed its back with UV rays for 2.5 minutes, and then, exposed its surface for 10 minutes to be fully cured. Consequently, the organic resin layer 311 is fabricated.

[0082] The adhesiveness of the metal oxide layer 302 is partly weakened in order to make it easier for layers to be separated. The partly wakening process of adhesiveness is carried out by irradiating laser light on the region that is to be peeled-off of the metal layer 301 or the oxide layer 303 along with the periphery thereof, or pressuring locally from outside on the region that is to be separated along with the periphery thereof for dam-

aging a part of the inside or the boundary face of the oxide layer 303. Specifically, a hard needle such as a diamond pen may be attached perpendicular to the region to be separated and moved along with the periphery thereof with applying loading. Preferably, a scriber device can be used to move with applying loading on the region with press force ranging from 0.1 to 2mm. It is important to carry out some processes for easy separating, that is, to prepare for separating process. Such preparatory process for weakening selectively (partly) the adhesiveness will prevent poor separating and improve the process yield.

[0083] By fabricating a first adhesive layer 312, a second substrate 313 can be bonded to the organic resin layer 311 via the first adhesive layer 312. As a material for fabricating the first adhesive layer 312, a known material that its adhesive can weaken by carrying out a predefined treatment in the following process can be used, however, the case that a photosensitive two-side tape that its adhesiveness weaken due to light irradiation is used in the following process will be described in this embodiment.

[0084] The second adhesive layer 314 is also fabricated over the exposed surface of the first substrate 300. The third substrate 316 is bonded thereto via the second adhesive layer 314. As a material for fabricating the second adhesive layer 314, a two-side tape is used same as the first adhesive layer 312. The third substrate 315 prevents the first substrate 300 from damaging in the following separating process. For the second substrate 313 and the third substrate 315, the substrate that has higher rigidity than that of the first substrate 300, for example, a quartz substrate or a semiconductor substrate, is preferably to be used.

[0085] The first substrate 300 provided with the metal film 301 is separated from the side of the region, which is partly weakened its adhesiveness, by a physical means. The metal layer 301 and the substrate 300 can be separated by splitting-off the metal oxide layer 302 with comparatively small force (for example, man's hand, air pressure of gas sprayed from a nozzle, ultrasonic waves, or the like). Specifically, the first substrate 300 can be separated by splitting-off a tungsten oxide layer, an interface between a tungsten oxide layer and a silicon oxide layer, or an interface between a tungsten oxide layer and a tungsten film. Thus, the device formative layer 250 formed over the oxide layer 303 can be separated from the first substrate 300. Fig. 3C shows a state of after separating process.

[0086] A portion of the metal oxide layer 302 is remained over the surface exposed by separating. The remained metal oxide layer 302 may hinder the bond between the exposed surface and the substrate or the like, so that the remained metal oxide layer 302 is preferably removed. For removing the remained metal oxide layer 302, aqueous alkali such as aqueous ammonia or aqueous acids can be used. In addition, the following process may be carried out at the temperature (at most 430°C) which mekes it easier for the portion of the metal oxide layer 302 to be separated.

[0087] Reference numeral 401 in Fig. 4A shows the state that is obtained by removing the remained metal oxide layer 302. In the following process, in case of fabricating another device formative layer over the device formative layer pasted to a thermal conductive substrate, this state of device formative layer (401) is used for the above described another device formative layer.

[0088] Next, a third adhesive layer 316 is fabricated, and a fourth substrate (a thermal conductive substrate) 317 is bonded to the oxide layer 303 (and a device formative layer 250 etc.) via the third adhesive layer 316 (Fig. 4A). Note that it is important that the adhesiveness of the second substrate 313 and the organic resin layer 311 bonded by the first adhesive layer 312 is greater than that of the oxide layer 303 (and the device formative layer 250 etc.) and the fourth substrate 317 bonded by the third adhesive layer 316.

[0089] As a fourth substrate (a thermal conductive substrate) 317, a glass substrate, a quartz substrate, a ceramic substrate, a silicon substrate, a metal substrate, or a stainless substrate, or the like, can be used. It is preferably to use a substrate having high thermal conductivity. Especially, it is preferably to use a ceramic substrate that contains aluminum oxide (alumina), aluminum nitride, aluminum nitride oxide, or silicon nitride as its main components. It is necessary that wirings for connecting electrically to a device formative layer which is stacked afterward is formed in the fourth substrate 317. As a means of forming the wirings, a known means that is used in the field of LSI for forming wirings in the substrate (also referred to as a die) on which chip is pasted can be used, so that the explanation thereof will be omitted.

[0090] A flattening film may be fabricated for preventing the device destruction and interconnection destruction in the device formative layer 250 due to irregularities of the surface of the fourth substrate 317 considering that the device formative layer according to the present invention is such a thin film having a thickness of at most 50μm.

[0091] As a material for the third adhesive layer 316, various curing adhesives such as a photo-curing adhesive, for example, a reaction-curing adhesive, a thermal-curing adhesive, or a UV-curing adhesive, or an anaerobic adhesive can be used. More preferably, the curing adhesives is given high thermal conductivity by means of mixing powder comprising silver, nickel, aluminum, or aluminum nitride, or filler.

[0092] Then, UV light is irradiated from the side of the second adhesive layer 313 in order to weak the adhesiveness of the two-sided tape, secondly, the second substrate 313 is separated form the device formative layer 250 etc. (Fig. 4B). And thirdly, the first adhesive layer 312 and the organic resin layer 311 are melted and removed by water washing the exposed surface.

[0093] A thermal conductive layer 318 is fabricated

over an insulating film that is exposed its surface. The thermal conductive layer 318 may be formed of a film of aluminum nitride, aluminum nitride oxide, diamond like carbon (DLC), or the like by vapor film formation method such as sputtering, reactive sputtering, ion beam sputtering, ECR (electron cyclotron resonance) sputtering, ionization vapor deposition, or the like.

[0094] Fig. 4C shows a state that is obtained by fabricating the thermal conductive layer 318.

[0095] Next, a fourth adhesive layer 319 is fabricated over the thermal conductive layer 318. Here, another device formative layer having a state of 401 obtained up through the process of Fig. 4A is bonded via the fourth adhesive layer 319 (Fig. 5A). In addition, another device formative layer having a state of 401 is referred to as a second device formative layer 501, and the device formative layer that is fabricate over the fourth substrate 317 is referred to as a first formative layer 502.

[0096] An organic resin layer 320, a fifth adhesive layer 321, and the fifth substrate 322 are fabricated over the second device formative layer 501. In the case of this embodiment, a device formative layer in an upper portion (501 illustrated in Fig. 5A) is necessary to be small in order not to cover an electrode pad of a device formative layer by forming the lamination structure.

[0097] Then, UV light is irradiated from the side of the fifth adhesive substrate 322 in order to weak the adhesiveness of the two-sided tape used as the fifth adhesive layer 321, and then, the fifth substrate 322 is separated form the second device formative layer 501 (Fig. 5B). Further, the fifth adhesive layer 321 and the organic resin layer 320 are melted and removed by water washing the exposed surface.

[0098] Thus, a structure in which the first device formative layer 502 and the second device formative layer 501 are stacked as shown in Fig. 5C can be formed. Within the structure shown in Fig. 5C, electrode pads (323, 324) of each device formative layer and wirings (not shown) that are provided in advance with the fourth substrate 317 having thermal conductivity are connected by a connection wire, and so the structure shown in Figs. 1A to 1C can be formed. The connection wire may be formed of Au, Cu, Al-Si, or Au alloys.

Embodiment 2

[0099] In this embodiment, a method for manufacturing a semiconductor chip according to the present invention that has a structure described in Embodiment Mode 2 will be explained in detail with reference to Figs. 6A to 8C.

[0100] Fig. 6A shows the state that the structure having a metal layer 601, a metal oxide layer 602, an oxide layer 603, a device formative layer 604 including a plurality of TFTs or wiring, an organic resin layer 611, a first adhesive layer 612, a second substrate 613, each of which is fabricated over a first substrate 600 is formed. In addition, a third substrate 615 is pasted on the first substrate 600 via a second adhesive layer 614 which is in contact with the first substrate 600 is formed, and the metal oxide layer 602 between the metal layer 601 and the oxide layer 603 is split-off. This structure is formed by the same manner and the same material as that described in Embodiment 1 and will not be further explained here. A portion of the metal oxide layer 602 is remained over the surface exposed by separating. The remained metal oxide layer 602 may hinder the bond between the exposed surface and the substrate or the like, so that the remained metal oxide layer 602 is preferably removed. For removing the portion of the metal oxide layer 602, aqueous alkali such as aqueous ammonia or aqueous acids can be used. In addition, the following process may be carried out at the temperature (at most 430°C) which makes it easier for the remained metal oxide layer 602 to be separated.

[0101] After separating substrates and removing the remained a metal oxide layer 602, an opening portion 606 for reaching to a wiring 605 is formed from the side of the oxide layer 603 exposed to the surface by patterning using masks formed by photolithography.

[0102] Then, an auxiliary wiring is provided with the opening portion 616 to form the structure shown in Fig. 6C. As a material for forming the wiring, an element selected from the group consisting of Ag, Au, Ta, W, Ti, Mo, Al, or Cu, or alloys or compounds containing these elements as their main components can be used. Reference numeral 701 in Fig. 6C shows a state that is completed by forming an auxiliary wiring 617. In case of fabricating another device formative layer over the device formative layer pasted on the thermal conductive substrate in the following process, this state of device formative layer (701) is used for the above described another device formative layer.

[0103] Next, a third adhesive layer (anisotropic conductive adhesive layer) 618 is fabricated, and a fourth substrate (thermal conductive substrate) 619 is bonded to the oxide layer 603 (and the device formative layer 604 etc.) via the third adhesive layer 618 (Fig. 7A). Note that it is important that the adhesiveness of the second substrate 613 and the organic resin layer 611 bonded by the first adhesive layer 612 is greater than that of the oxide layer 603 (and the device formative layer 604 etc.) and the fourth substrate 619 bonded by the third adhesive layer 618.

[0104] As a fourth substrate (a thermal conductive substrate) 619, a glass substrate, a quartz substrate, a ceramic substrate, a silicon substrate, a metal substrate, or a stainless substrate, or the like, can be used. It is preferably to use a substrate having high thermal conductivity. Especially, it is preferably to use a ceramic substrate that contains aluminum oxide (alumina), aluminum nitride, aluminum nitride oxide, or silicon nitride as its main components. It is necessary that wirings for connecting electrically to a device formative layer which is stacked afterward is formed in the fourth substrate 619. As a means of forming the wirings, a known means

that is used in the field of LSI for forming wirings in the substrate (also referred to as a die) on which chip is pasted can be used, so that the explanation thereof will be omitted.

[0105] As a material for fabricating the third adhesive layer (anisotropic conductive adhesive layer) 618, adhesive which is made by dispersing an anisotropic conductive material on a photo-curing adhesive such as a reaction-curing adhesive, a thermal-curing adhesive, or a UV-curing adhesive, or an anaerobic adhesive can be used. As an anisotropic conductive material, metal particles such as Ag, Au, Al, or the like coated with insulating films and having a unidirectional conductivity can be used.

[0106] Then, UV light is irradiated from the side of the second adhesive layer 613 in order to weak the adhesiveness of the two-sided tape, and then, the second substrate 613 is separated form the device formative layer 604 (Fig. 7B). Further, the first adhesive layer 612 and the organic resin layer 611 is melted and removed by water washing the exposed surface.

[0107] A thermal conductive layer 620 is fabricated over an exposed surface of an insulating film. The thermal conductive layer 620 may be formed of a film of aluminum nitride, aluminum nitride oxide, diamond like carbon (DLC), or the like by vapor film formation method such as sputtering, reactive sputtering, ion beam sputtering, ECR (electron cyclotron resonance) sputtering, ionization vapor deposition.

[0108] Fig. 7C shows a state that is obtained by fabricating the thermal conductive layer 620.

[0109] Next, a fourth adhesive layer 621 is fabricated over the thermal conductive layer 620 shown in Fig. 7C. Here, another device formative layer having a state of 701 obtained up through the process of Fig. 6C is bonded thereto via the fourth adhesive layer 621 (Fig. 8A). In addition, another device formative layer having a state of 701 is referred to as a second device formative layer 801, and the device formative layer that is fabricated over the fourth substrate 619 is referred to as a first formative layer 802.

[0110] An organic resin layer 622, a fifth adhesive layer 623, and a fifth substrate 624 are fabricated over the second device formative layer 801. In the case of this embodiment, an electrode pad of a device formative layer is not used for connecting electrically as described in Embodiment 1, the wiring 805 of the first device formative layer 801 and an auxiliary wiring 825 of the second device formative layer 801 are electrically connected each other via the fourth adhesive layer (anisotropic conductive adhesive layer) 621, so that it is no problem that the sizes of each device formative layer are different from each other.

[0111] Then, UV light is irradiated in order to weak the adhesiveness of the two-sided tape used for the fifth adhesive layer 623 from the side of the fifth adhesive layer 624, and then, the fifth substrate 624 is separated from the second device formative layer 801 (Fig. 8B). Further, the fifth adhesive layer 623 and the organic resin layer 622 are melted and removed by water washing the exposed surface.

[0112] Thus, a structure in which the first device formative layer 802 and the second device formative layer 801 are stacked can be formed as shown in Fig. 8C. In this embodiment, the case that a semiconductor chip shown in Fig. 8C is formed by removing the organic resin layer, the fifth adhesive layer 623, and the fifth substrate 624 through the process shown in Fig. 8A is explained, but not exclusively, the structure obtained by bonding as shown in Fig. 8A can be used as a semiconductor chip.

Embodiment 3

[0113] In this embodiment, the structure of a semiconductor chip that has a different structure described in Embodiment 1 or 2 will be described with reference to Figs. 17A to 18B. The structure according to this embodiment is formed by stacking a plurality of device formative layers and bonding a device formative layer which is fabricated at the very end to a thermal conductive substrate. Such structure is different from the structure described in Embodiment 1 or 2 which is formed by bonding a first device formation layer to a thermal conductive layer and stacking a plurality of device formative layers sequentially.

[0114] As shown in Fig. 17A, a first device formative layer 1902 is fabricated over a first substrate 1800. Further, a second substrate 1815 is bonded to the first substrate 1800 via a second adhesive layer 1814.

[0115] In this embodiment, the first substrate 1800, the second adhesive layer 1814, and a second substrate 1815 is not separated by splitting-off a metal oxide layer 1802 at this point. A thermal conductive film 1820 is fabricated over a first device formation layer 1902 not to cover a wiring 1805. The thermal conductive film 1820 may be fabricated by using the same material and the same manner as the thermal conductive layer 620 in Embodiment 2.

[0116] A first adhesive layer 1821 is fabricated over the first device formative layer 1902 on which the thermal conductive film 1820 is fabricated, and a second device formative layer 1901 is bonded thereto. In addition, the first adhesive layer 1821 is an anisotropic conductive adhesive layer formed of an anisotropic conductive adhesive.

[0117] The device formative layer 1902, which is bonded here, has the same structure of the second device formative layer 801 shown in Fig. 8A in Embodiment 2. Thus, the device formative layer 1902 has an auxiliary wiring 1825 connected electrically to the wirings fabricated in the second device formative layer 1901, a third adhesive layer 1823, and a third substrate 1824. In addition, the auxiliary wiring 1825 is connected electrically to the wiring 1805 in the device formative layer 1902 via the first adhesive layer 1821.

[0118] After bonding the first device formative layer 1902 to the second device formative layer 1901, UV light is irradiated from the side of the third substrate 1824 in order to weak the adhesiveness of the two-sided tape used as the third adhesive layer 1823, secondly, the third substrate 1824 is separated form the second device formative layer 1901. And thirdly, the third adhesive layer 1823 and the organic resin layer 1822 are melted and removed by water washing the exposed surface.

[0119] A bump 1826 is formed over the surface of the second device formative layer 1901 in contact with the exposed wiring, and a fourth substrate 1827 having thermal conductivity is bonded thereto via a fourth adhesive layer 1828 formed of an anisotropic adhesive. As a material for forming the bump 1826, tungsten (W), tungsten-rhenium (W-Re), palladium (Pd), beryllium copper (BeCu), or the like can be used.

[0120] As a fourth substrate 1827, a glass substrate, a quartz substrate, a ceramic substrate, a silicon substrate, a metal substrate, or a stainless substrate, or the like, can be used. It is preferably to use a thermal substrate having high thermal conductivity. Especially, it is preferably to use a ceramic substrate that contains aluminum oxide (alumina), aluminum nitride, aluminum nitride oxide, or silicon nitride as its main components. A wiring for electrical connections via the wirings of the second device formative layer 1901 and the bump 1826 is necessary to be formed. As a means of forming the wirings, a known means that is used in the field of LSI for forming wirings in the substrate (also referred to as a die) on which chip is pasted can be used, so that the explanation thereof will be omitted. Fig. 17B shows the state that the lamination structure of a device formation layer shown in Fig. 17A is reversed.

[0121] The first substrate 1800, the second adhesive layer 1814, and the second substrate 1815 are separated by splitting-off the metal oxide layer 1802 between the metal layer 1801 and the oxide layer 1803 by the same way described with reference to Fig. 6A in Embodiment 2.

[0122] In this embodiment, the metal oxide layer 1802 remained over the second device formative layer 1901 is removed by using aqueous alkali such as aqueous ammonia or aqueous acids. This removing treatment may be carried out according to need.

[0123] Thus, a structure, which is different from that described in Embodiment 1 or 2, in which the second device formative layer 1902 and the second device formative layer 1901 are stacked over a thermal conductive substrate (the fourth substrate 1827) can be formed as shown in Fig. 18B.

Embodiment 4

[0124] In this embodiment, a specific structure in which a device composed of TFTs included in a plurality of device formative layers stacked over a thermal conductive layer can be electrically connected to the outside via a wiring formed in a thermal conductive layer and solder balls 910 and 920 within a semiconductor chip according to the present invention comprising a plurality of device formative layers over a thermal conductive substrate will be described with reference to Figs. 9A and 9B. Fig. 9A shows a structure of the semiconductor chip described in Embodiment Mode 1. Fig. 9B shows a structure of the semiconductor chip described in Embodiment Mode 2.

[0125] Fig. 9A shows a semiconductor chip having an interconnection structure of wire bonding. An electrode pad 911 connected electrically to a wiring of each device formative layer 901 is connected electrically to a thermal conductive substrate 906 by a connection wire 909 in the semiconductor chip. The device formative layer 901 is formed by the same way described in Embodiment 1.

[0126] A wiring 907, which penetrates the substrate, is formed in the opening portion of the thermal conductive substrate 906. An insulating layer 908 is fabricated over the both surface of the thermal conductive substrate with leaving a part of these wirings 907.

[0127] The wiring 907, which is not covered by the insulating layer 908, is connected electrically to the electrode pad 901 of each device formative layer via the connection wire 909. The solder ball 910 is formed over the face of the thermal conductive layer 906 which is not bonded with the device formative layer 911.

[0128] Electrical interconnection can be obtained by pasting the semiconductor chip shown in Fig. 9A on a wiring board (printed wiring board) with aligning so as the wirings on the wiring board to be in contact with the solder ball 910.

[0129] The semiconductor chip shown in Fig. 9B has an interconnection structure of flip chip. A wiring and an auxiliary wiring of each device formative layer 931 are electrically connected each other by an anisotropic conductive adhesive layer. In the device formative layer 931 described in this embodiment, a plurality of wirings are leaded out by a leading out wiring 921, a bump 928 is formed in contact with the leading out wiring 921, and the bump 928 is electrically connected to the wiring 917 via an anisotropic conductive adhesive layer 915 as shown in the bottom side of Fig. 9B, which is an enlarged view of 923 in the upper side of Fig. 9B. This structure is different from that described in Embodiment 2.

[0130] As a material for fabricating the anisotropic conductive adhesive layer 915, the same material for the anisotropic conductive adhesive layer in Embodiment 2 can be used. That is, the anisotropic conductive adhesive layer 915 is formed of an anisotropic conductive particle 925 made of metal particles such as Ag, Au, Al, or the like coated with insulating films and having a unidirectional conductivity and an adhesive 924 such as a photo-curing adhesive, for example, a reaction-curing adhesive, a thermal-curing adhesive, or a UV-curing adhesive, or an anaerobic adhesive. The bump 928 and the wiring 917 can be electrically connected via anisotropic conductive particle 925.

[0131] Over a thermal conductive substrate 916 on which a device formative layer is stacked, a solder ball 920 formed of a conductive material is formed in contact with the wiring 917 penetrating the substrate and the insulator 918 is formed in the opening portion as in the case of Fig. 9A.

[0132] Electrical interconnection can be obtained by pasting the semiconductor chip shown in Fig. 9B on a wiring substrate (printed wiring board) with aligning so as the wirings on the wiring substrate to be in contact with the solder ball 920.

Embodiment 5

[0133] An operation and a structure of a chip pasted over a thermal conductive substrate in case that the chip has a function as a CPU will be described with reference to Fig. 10 in this embodiment.

[0134] When an opcode is inputted to an interface 1001, the code is decrypted in an analysis unit 1003 (also referred to as an Instruction Decoder), and a signal is inputted to a control signal generation unit 1004 (a CPU Timing Control). Upon inputting the signal, a control signal is outputted from the control signal generation unit 1004 to an arithmetic logical unit 1009 (hereinafter, an ALU) and a register unit 1010 (hereinafter, a Register).

[0135] The control signal generation unit 1004 comprises an ALU controller 1006 for controlling the ALU 1009 (hereinafter, ACON), a unit 1005 for controlling the Register 1010 (hereinafter, a RCON) , a timing controller 1007 for controlling timing (hereinafter, a TCON), and an interruption controller 1008 for controlling interruption (hereinafter, an ICON).

[0136] On the other hand, when an operand is inputted to the interface 1001, the operand is outputted to the ALU 1009 and the Register 1010. Then, a processing such as a memory read cycle, a memory write cycle, an I/O read cycle, an I/O write cycle, or the like, based on a control signal, which is inputted from the control signal generation unit 1004, is carried out.

[0137] The Register 1010 is composed of a general resister, a stack pointer (SP), a program counter (PC), or the like.

[0138] An address controller 1011 (hereinafter, ADRC) outputs 16 bits address.

[0139] A structure of CPU described in this embodiment is illustrative only as a CPU included in the semiconductor chip according to the present invention and does not limit the structure of the present invention. Therefore the semiconductor chip according to the present invention can be completed by using a known CPU with the structure other than that of the present invention.

Embodiment 6

[0140] The structure of a semiconductor chip in which a CPU and a light-emitting device are stacked will be described with reference to a cross-sectional structure in Fig. 11 A first device formative layer 1102 fabricated over a thermal conductive layer 1101 comprises a CPU. A second device formative layer 1103 comprises a light-emitting apparatus. And these layers are connected each other by a connection wire 1104.

[0141] The CPU included in the first device formative layer 1102 can adopt the structure described in Embodiment 4 and will not be further explained.

[0142] The light-emitting apparatus included in the second device formative layer 1103 is composed of a drive circuit portion 1107 (a source side drive circuit or a gate side drive circuit) formed of a CMOS circuit which is a combination of n-channel TFTs 1105 and p-channel TFTs 1106, and a pixel portion 1108.

[0143] In addition, a TFT for forming a drive circuit may be formed of a known CMOS circuit, PMOS circuit, or NMOS circuit. A driver integrated type formed by forming a drive circuit portion and a pixel portion over one device formative layer is described in this embodiment, but not exclusively, the drive circuit portion may be stacked over another device formative layer.

[0144] The pixel portion 1108 is composed of a plurality of pixels including a switching TFT 1111, a current control TFT 1112, and a first electrode 1113 connected electrically to the drain of the current control TFT 1112. An insulator 1114 is formed to cover the edge portion of the first electrode 1113.

[0145] An electroluminescent device 1117 is composed of a first electrode 1113, a second electrode 1116, and an electroluminescent layer 1115 which is interposed between these electrodes. As a material for forming the first electrode 1113, a material having large work function is preferably used. For example, a single layer such as a titanium nitride film, a chrome film, a tungsten film, a Zn film, or Pt film; a lamination layer of a titanium nitride film and a film containing aluminum as its main components; or a three lamination layer of a titanium nitride film, a film containing aluminum as its main components, and a titanium nitride film, are useful. By forming the first electrode to have a lamination structure, resistance as a wiring can be low, good properties of ohmic contact can be obtained, and the first electrode can serve as an anode.

[0146] The electroluminescent layer 1115 can be fabricated by vapor deposition using an evaporation mask or ink-jetting.

[0147] As a material for the second electrode (cathode) 1116 formed over the electroluminescent layer 1115, a small work function material (Al, Ag, Li, Ca, or alloy of these materials such as MgAg, MgIn, AlLi, CaF_2, or CaN) is useful. Here, the second electrode (cathode) 1116 is formed of a lamination of a thin metal film, a transparent conductive film (Indium-tin-oxide (ITO), indium oxide-zinc oxide (In_2O_3-ZnO), zinc oxide (ZnO), or the like) in order light to pass through the second electrode.